A Novel MMIC *X*-Band Phase Shifter

KEN WILSON, JONATHAN M. C. NICHOLAS, GARY MC DERMOTT, AND JOHN W. BURNS

Abstract—**A novel configuration for monolithic phase shifters is presented. The layout and fabrication of a single chip, four-bit *X*-band phase shifter, measuring 3.7×2.3 mm, is described in some detail. The first samples to be assessed exhibited full 360° coverage at the design frequency, operation throughout *X*-band, good matches, and an insertion loss less than 5 dB.**

I. Introduction

THE potentially large-volume requirement for components for phased-array radar systems has stimulated a number of developments of monolithic phase shifting elements on GaAs [1]–[4]. As with any high-quantity application, cost is a major factor, and this, for a monolithic circuit, means small chip area, undemanding processing, and a high degree of integration.

This paper describes a single chip, four-bit, *X*-band phase shifter which measures only 3.7×2.3 mm. It gives 16 states at nominal 22.5° increments with an insertion loss of less than 5 dB and is fabricated with a relatively undemanding 2-μm technology. Having an equivalent gate width of under 1 mm and an area of about 9 mm^2, this chip compares favorably with previously reported circuits in terms of complexity and size. The four-bit, *X*-band phase shifter of [1] has total gate periphery of 9.6 mm and an area of 51 mm^2; another circuit [3] uses 30 mm^2 for the same function, and a further design [2] for a vector modulator with similar phase-setting accuracy, albeit at *S*-band, consists of 11 chips with a total area of about 30 mm^2.

The circuit configuration is believed to be entirely novel and, as it consists of a moderate number of identical simple sections, it is well suited to a monolithic construction.

II. Circuit Configuration and Basic Design Considerations

The basic circuit is shown in Fig. 1. It consists of a 90° coupler of which ports 1 and 4 are the RF input and output, and ports 2 and 3 are each connected to a transmission line along which are tapped a number of shunt switches to ground.

All switches are normally open except for one pair. An input signal applied to port 1 of the coupler will split equally between the two transmission lines, reflect from the closed switch pair, and recombine in the coupler to appear at the output, port 4. The phase is controlled by the choice of which switch pair to close. Loads are provided at the remote ends of the tapped lines to absorb any leakage past the switches.

Being a simple configuration, the circuit analysis required for a prototype design is not difficult; the approach is outlined in the Appendix. A number of practical decisions then have to be made.

The first concerns the choice of switch. The Appendix shows that this needs to have an off-state capacitance of 0.05 pF or less (it can always be artificially increased). It also needs an on-state resistance very much less than 50 Ω to achieve a low return loss; a resistance R_{on} of 6 Ω would give ~2-dB return loss. This CR product of 0.3 ps (or cutoff frequency of 530 GHz) is at least one order of magnitude beyond the capability of the best FET switches. Schottky diodes, which can meet the requirement if suitably designed, have therefore been chosen for the switching devices, although p-i-n diodes [5] are preferred for future high-power versions. The Schottky diodes are produced using selective area ion implantation, thus permitting future integration with FET-based circuits.

Power handling of this circuit using Schottky-diode switches is limited by the ability of the diodes to withstand the RF voltage in the off-state or to carry the RF current in the on-state; the former is governed by breakdown voltage and the latter by electromigration in the Schottky contact. Both are dependent on bias conditions. The diodes employed here are designed to run at −3 V or +30 mA to give a power-handling capability for the circuit of at least 30 mW, so receiver local oscillators and transmitter drivers can therefore both be controlled by this chip. The bias or control signals are conveniently applied across decoupling capacitors located in series with the RF grounded ends of the diodes and returning via the loads terminating the tapped lines.

Insertion-loss predictions for the circuit are relatively simple to make. The return loss of the "on" diodes will be 2 dB for a 6-Ω diode resistance and 1.5 dB will result from the two passes through the coupler. This 3.5-dB subtotal will be state independent assuming all diodes to be identical. Other loss contributions arise from the series resistances of the "off" diodes (0.01 dB/diode), loss in the decoupling capacitors and to the bias circuit (< 0.01 dB/section), and series resistance in the inductive elements (0.013 dB/section) giving a state dependent loss of 0.5 dB. The overall loss should be ~4 dB.

The final basic design consideration is bandwidth. Lange couplers (the obvious choice) have a near-octave band-

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The authors are with GEC Research Limited, GEC Hirst Research Centre, East Lane, Wembley, Middlesex HA9 7PP, England.

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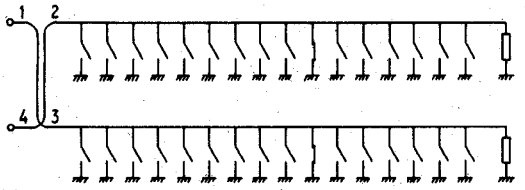


Fig. 1. The basic circuit.

width and the tapped delay lines, (which, as will be discussed further, are virtually lumped artificial lines) have a cutoff frequency around 50 GHz. This circuit should therefore be very acceptable for use over the whole of *X*-band although it must be recognized that it is a time-delay circuit and, hence, the phase shift will be proportional to frequency within this band. A time-delay characteristic is, in fact, preferred for phased-array applications [6].

Having considered the main characteristics to be expected from this new circuit, it is appropriate now to mention some other points of interest.

III. The New Circuit–Other Points of Interest

The element values for the prototype four-bit circuit are calculated in the Appendix, the series elements being of ~100-Ω characteristic impedance and ~0.017 of a wavelength long. These will behave as almost ideal inductances and the tapped-line structure will thus behave as an artificial line. A size advantage is realized with the physical length of the tapped line being only half the electrical length. One limitation of the circuit in its present form is the difficulty of extension to more bits or much higher frequencies as the demands on switch capacitances become very severe; however, integrated p-i-n diodes currently under development [5] could ease this problem and simultaneously increase the power-handling capability and further reduce the insertion loss.

Although a five-bit *X*-band version of the current circuit looks impractical for the above reasons, there is another way of achieving fine control of the phase by using the circuit already described in a different mode of operation. If the final pair of diodes in the circuit is permanently biased to the on-state and the reverse bias on all others is varied simultaneously, then the propagation constant of the artificial line will change as a consequence of the variation in the diode capacitances. For the type of diodes to be described, a capacitance variation of ~20 percent can be expected, giving a continuous phase control of ~10 percent or ~36°. Two identical chips, one digitally controlled and one with analog control, could therefore give complete phase coverage.

Considerations of the propagation constant of the artificial line also enable predictions of phase stability with temperature to be made. There are two effects: the first is thermal expansion of the GaAs, which is not significant, and the second is the temperature dependance of the diode capacitance, which is significant. The latter results from changes in the barrier voltage with temperature of ~2.5 mV per °C. At 3-V (applied) reverse bias, the barrier

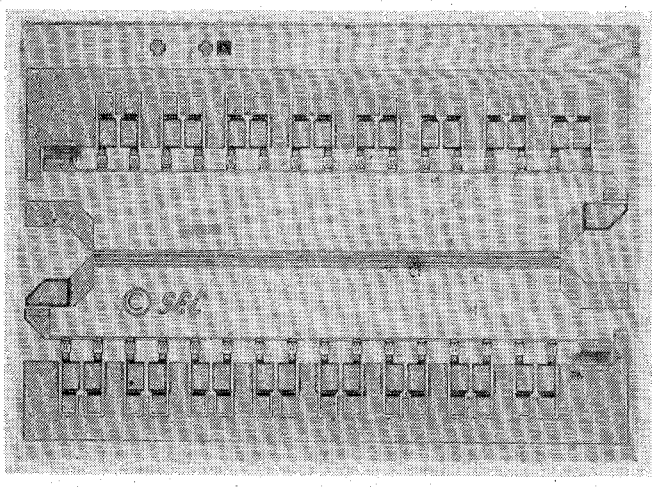


Fig. 2. The four-bit *X*-band phase shifter chip. The chip size is 3.7×2.3 mm.

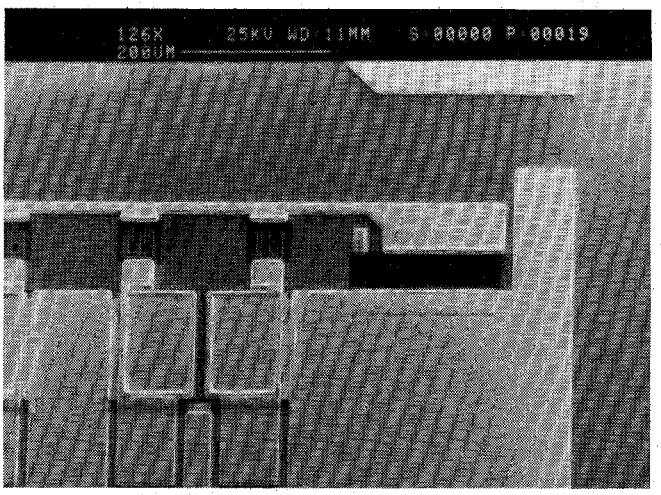


Fig. 3. Detail of the phase shifter chip.

potential should therefore change by 0.068 percent/°C; thus, the diode capacitance should change by 0.034 percent/°C and the line phase shift by 0.017 percent/°C. The maximum effect would be seen when the circuit is set for maximum delay and should be ~0.06 degrees of angle per °C.

IV. Detailed Design and Layout

Owing to the compact size of this circuit, it was realized that parasitic effects would be important. These were thoroughly investigated with the aid of scale modeling techniques before the circuit was laid out on GaAs. A picture of the final layout of this circuit on GaAs is shown in Fig. 2, and a close up of two sections, and the dummy load, is shown in Fig. 3. With reference to the latter, we can identify the following parasitics which will be expected to modify the basic design:

1) fringing capacitance in shunt with the diode,
2) the effects of the microstrip "T" junction,
3) inductance in series with the diode,
4) modification of the microstrip transmission-line parameters by the presence of the ground strip.

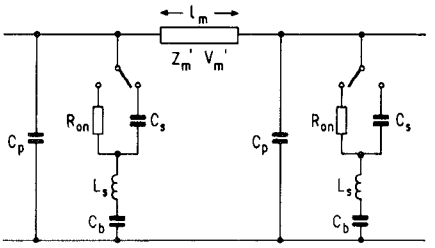


Fig. 4. Circuit diagram including parasitic components.

When the circuit is laid out on GaAs, some fringing capacitance is expected to exist in parallel with the diode. This will consist of capacitance between the section of line at the "top" end of the diode and the grounded strip as well as the ground plane; there will also be some fringing associated with the diode structure close to the diode fingers. These effects were estimated theoretically and verified by the use of scale modeling as follows. A model was made on a block of material with dielectric constant 13, 2 cm thick, to represent the 200-μm GaAs substrate. The metal pattern was laid out on the surface 100 times the dimensions proposed for the MMIC and the measurements were made at 100 MHz. The fringing capacitance of the diode itself was measured by making a somewhat larger model; as the diode is very small compared to the substrate thickness, the ground plane was not included. It was found that the overall parasitic was quite significant, representing some 15 percent of the diode capacitance. It is represented in the full-circuit diagram of Fig. 4 by C_p.

The microstrip "T" junction has been well analyzed, in the context of hybrid microwave circuits, by Gopinath *et al.* [7], [8]. They found it adequately represented by a shunt capacitor and an inductance in series with each of the three arms. In this circuit, the capacitor may be ignored, as its value is much less than the parasitic mentioned above, and the inductors may be represented by small lengths of line each of length Δl. This effect may be allowed for in the final layout by adjusting the length of each microstrip section by $2\Delta l$.

The inductance in series with the diode (L_s) may simply be estimated as that associated with the short length of microstrip line containing it. It was discovered that the effect on performance is quite serious if the line is too long. For this reason, the transmission-line sections were placed quite close to the ground strip; this in itself was found to cause a parasitic effect, but one which could more easily be allowed for. The effect which would be expected is a reduction in the inductance per unit length L and an increase in capacitance C, compared to the line with no ground strip. These effects were quantified by the use of a $100\times$ scale model of the transmission line, as described above, and the effect was allowed for by reworking the calculations described in the Appendix using the modified values of L and C

A scale model was then made of one arm of the structure, with thirteen sections; it was designed including all parasitic effects mentioned above. The diodes in the "on" and "off" states were modeled with discrete resistors and

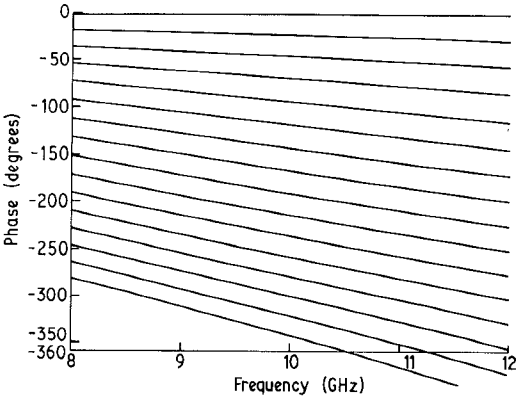


Fig. 5. Predicted phase versus frequency for each state.

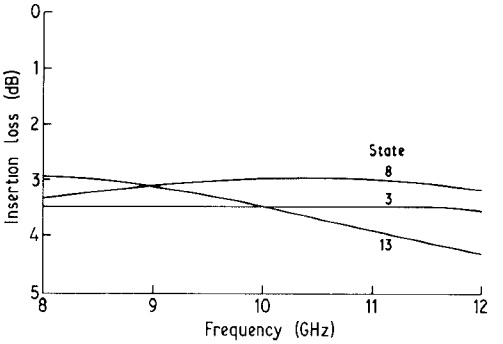


Fig. 6. Predicted insertion loss versus frequency for three arbitrary states.

capacitors, respectively, and the reflection coefficient of the circuit was measured, at the scale frequency, for each state. Very good agreement was obtained with the design performance.

A high-isolation coupler is required for this circuit as any leakage of unmodulated signal from input to output will, clearly, degrade the phase response. The isolation of the Lange coupler can be improved by using tighter coupling [9]; the penalties are a slight imbalance in drive to the two arms and an increased resistive loss owing to the narrower tracks required. The coupler used has a strip width of 10 μm and a separation of 18 μm, giving a predicted loss of 0.7 dB and isolation of around 30 dB. This isolation is not possible to measure accurately; however, it can be deduced from the overall circuit performance that it is fairly close to the design rules.

Figs. 5 and 6 show the predicted phase shift and insertion loss of the phase shifter chip, including the Lange coupler. The circuit of Fig. 4, which includes the effect of the parasitics described above, was used for the analysis with component values as given in Table I.

V. Device Fabrication

The required structure to realize the diode is a low-doped surface region with a buried n^+ layer to reduce the series resistance. Active regions for the diodes and resistors are defined in undoped semi-insulating GaAs substrates by selective area Si ion implantation to give a planar surface and the required profile.

TABLE I
COMPONENT VALUES

C_S, R_{on}	Diode parameters	0.044 pF, 6 Ω
l_m	Line length	0.17 mm
Z_m*	Line impedance*	101 Ω
V_m*	Phase velocity*	1.12×10^{10} cm/s
C_p	parasitic capacitance	0.0055 pF
L_s	Series inductance	100 pH
C_b	dc blocking capacitor	10 pF

*These values modified owing to the proximity of the ground strip (see text).

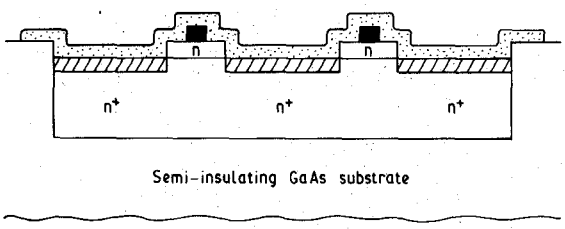


Fig. 7. Cross section showing the diode structure.

In the regions requiring low-resistance contacts, the surface is etched back to the buried n^+ region immediately prior to depositing the metallization; these contacts are then alloyed. The 2-μm-wide Ti/Au Schottky fingers are then defined by conventional photolithography on the lightly doped surface to produce the interdigitated diode structure which can be seen in the photograph of Fig. 3. A cross section of the diode is shown in Fig. 7. The same metallization stage also defines the bottom plate of the capacitors and the lower cross connections for the Lange coupler.

Dielectric for the capacitors and diode passivation is provided by Si_3N_4 deposited by plasma-enhanced chemical vapor deposition. Supports for the airbridge connections onto the top plates of the capacitors, and between the arms of the Lange coupler, are defined in resist (ultimately removed); this is followed by the evaporation of the seed metals for plating. The top plates of the capacitors and the rest of the circuit are then defined in a further layer of photoresist and plated. The plating schedule has been optimized in order to give low bulk resistance and maximum yield of airbridges (there are 68 in this circuit). After removing this photoresist, the seed metals are removed from the unplated areas. Following substrate thinning to 200 μm, the reverse side is metallized and the discrete chips separated by sawing.

VI. RF ASSESSMENT

A. Test Hardware

RF evaluation of the phase shifter chip requires the application of 16 independent control signals each capable of supplying up to 5-V reverse bias and 100-mA forward current to the appropriate diode pair. To facilitate connection to microwave network analysis and the purpose built dc control hardware, a test mount has been developed which mates directly with readily available APC 3.5-mm coaxial to microstrip RF launchers and 0.1-in in-line printed circuit edge connectors. It comprises an alumina substrate, 2 in $\times$ 1 in $\times$ 0.020 in, into the center of which is inserted a gold-plated metallic chip support. The support provides a continuous RF ground between the chip and the alumina substrate and incorporates longitudinal side ridges for tape or stitch bonding to the on-chip ground contact pads; future versions may incorporate on chip grounding with through-chip via holes to simplify the external connections. The chip is mounted on the support with a thin film of conducting epoxy, and gold wire is thermocompression-bonded between the on-chip dc and RF contact pads and the corresponding thin-film feeder lines on the alumina substrate.

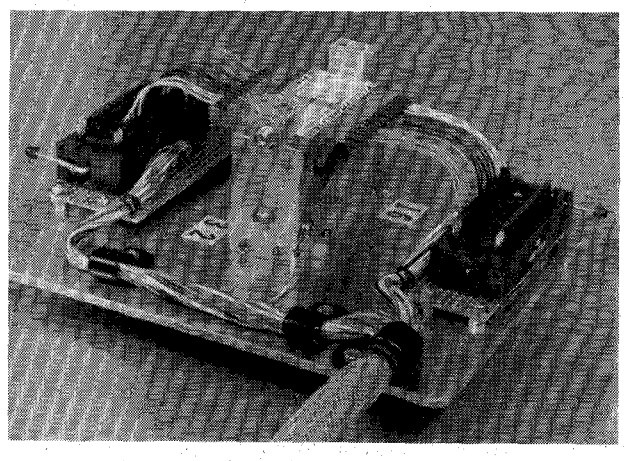


Fig. 8. The phase shifter test assembly.

Fig. 8 shows the test assembly. The 50-Ω microstrip feeder lines are maintained in intimate contact with the coaxial launcher assemblies by spring-loaded metallic supports located directly beneath each launcher; these also provide a continuous RF ground between the alumina substrate and the test fixture. The assembly is designed to place minimal mechanical stress on the package in order to ensure optimum reliability and repeatability of the coaxial-microstrip interface. The arrangement described is for test purposes only; in eventual use, the phase shifter chip would be mounted adjacent to a Si IC driver (it is TTL compatable) and addressed with, at most, four control lines.

B. Results

This section presents the results of RF assessment on several 16 state phase shifter chips at *X*-band. Operating bias conditions, unless otherwise stated, were 3-V reverse bias in the "off" state, and 30-mA forward current per diode in the "on" state.

Fig. 9 shows the transmission phase as a function of frequency for each state. The divergence of the traces is consistent with the fixed time-delay nature of the circuit. The average phase shift per state is 22.5° at 8 GHz which, while enabling full 360° coverage throughout *X*-band, is slightly higher than was intended. The nonuniformity of the phase state characteristic is a function of diode capaci-

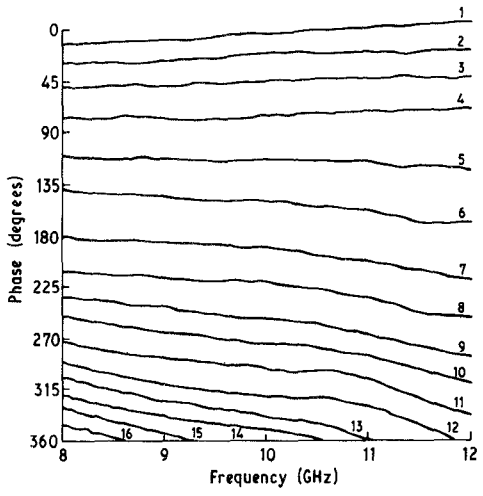


Fig. 9. Measured phase versus frequency for each state.

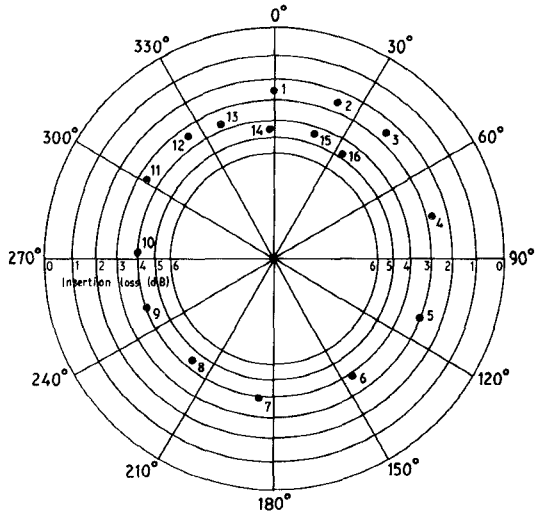


Fig. 10. Measured insertion loss for each state at 10 GHz.

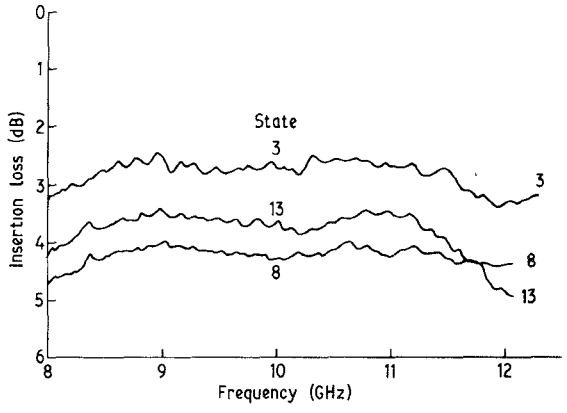


Fig. 11. Measured insertion loss versus frequency for three arbitrary states.

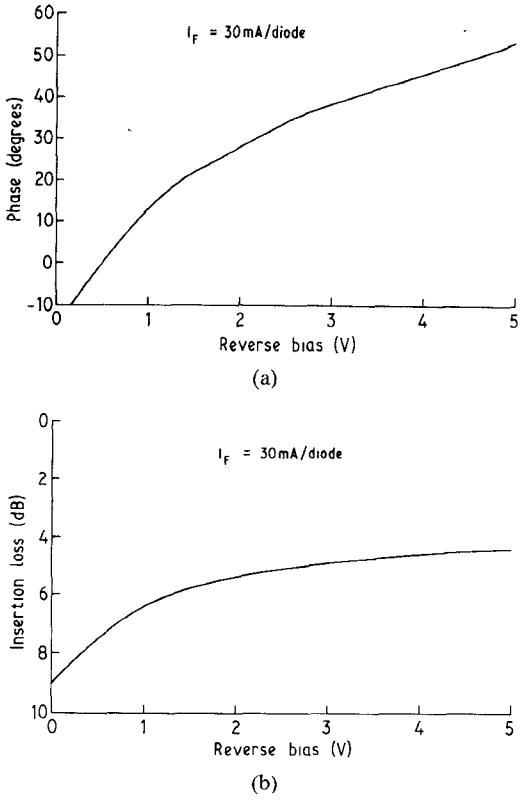


Fig. 12. Measured phase and insertion loss versus bias voltage.

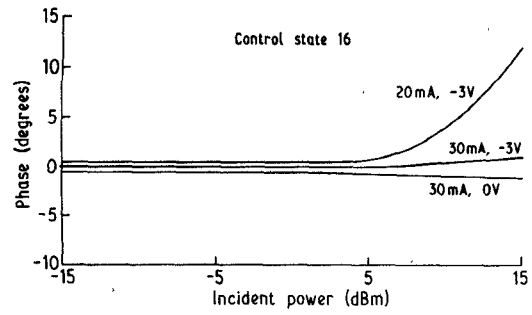
tance and is discussed below. Fig. 10 is a polar plot of insertion loss for each state at 10 GHz. Measured loss correlates well with the design performance, being less than 5 dB for all states over the frequency range 8–12 GHz; the frequency response for three arbitrary states is presented in Fig. 11. Return loss is typically 20 dB and is better than 15 dB for all states over the design bandwidth.

The nonuniformity of the phase characteristic can be explained as follows. Measurements on test structures revealed that the diode capacitances for all the first circuits assessed were high, by as much as 40 percent. It can be seen from the equations given in the Appendix that the effect of this is to reduce both the propagation velocity and the characteristic impedance of the artificial transmission lines. The reduction in line impedance from 50 Ω results in mismatches at the junction between the coupler and the lines which cause reflected signals in addition to those caused by the two "on" diodes. The net result is an error in mean phase shift, and a ripple in the actual phase shift for each state.

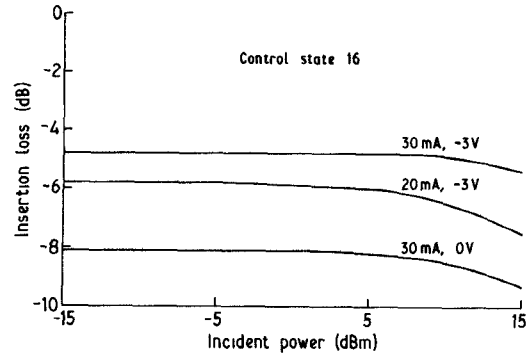
Simulations have shown that a good prediction of the measured results can be obtained by altering only the diode capacitance to this measured value. A high degree of correction is, therefore, confidently expected in future batches. It is also a measure of the tolerant nature of the basic design that a gross deviation in one component value has yielded a still attractive performance.

Fig. 12 shows the variation of transmission characteristics with reverse bias voltage, at 10 GHz, for the 16th state. Between 2 V and 5 V, a phase change of approximately 30° is obtained with a corresponding change in insertion loss of 1 dB. This illustrates the possibility, mentioned above, of using this circuit as an analog phase shifter.

The power handling capability of the circuit is indicated in Fig. 13. At the bias levels used for the measurements



(a)



(b)

Fig. 13 Measured phase and insertion loss versus input power.

described above, the power performance is limited by the current flowing through the "on" diode pair rather than by voltage. It can be seen that the performance is degraded when the bias current is reduced to 20 mA. At 30 mA, however, the device can comfortably handle 15-dBm (30-mW) input power with a gain compression of only 0.5 dB and a phase response within 1.5° of the small-signal case.

VII. Conclusion

We have described a novel circuit configuration for monolithic phase shifters. This has been illustrated by the design and fabrication of a single-chip 16 state (four-bit) phase shifter intended for use at *X*-band. First samples of this circuit have exhibited the following performance:

frequency	*X*-band
phase shift	16 states at $22\frac{1}{2}°$ (i.e., 4-bit)
insertion loss	< 5 dB
return loss	>15 dB
bandwidth	8–12 GHz
analog mode phase shift	~ 30°
power handling	30 mW
chipsize	3.7×2.3 mm.

This performance is attractive and in good accordance with theoretical predictions.

Acknowledgment

This work owes much to our colleagues at the Hirst Research Centre, in particular: D. C. Bartle, for materials research; A. C. Bach, who designed and constructed the controller; and S. L. Singh for the scale modeling.

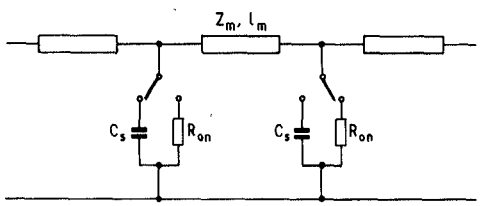


Fig. 14. One section of the phase shifter circuit.

Appendix
Analysis of the Basic Circuit

Phase Shift Increments and Impedance

Fig. 14 represents a portion of one of the tapped lines in the complete phase shifter. We first need to choose the length l_m and the characteristic impedance Z_m of the series transmission-line elements so that when loaded by the off-state capacitance of the switches the overall characteristic impedance is 50 Ω. Also, the transmission phase shift per section needs to be half the smallest phase increment required from the complete circuit since the signal traverses each section twice.

From the basic equations for characteristic impedance and propagation velocity, we can write

$$Z_m = \sqrt{L/C} \quad (\Omega) \tag{A1}$$

$$V_m = 1/\sqrt{L/C} \quad (\text{cm/s}) \tag{A2}$$

$$Z_0 = \sqrt{L \cdot l_m/(C \cdot l_m + C_s)} \quad (\Omega) \tag{A3}$$

$$V_0 = l/\sqrt{L \cdot l_m (C \cdot l_m + C_s)} \quad (\text{sections/s}) \tag{A4}$$

where

- Z_m characteristic impedance of series elements,
- V_m propagation velocity in series elements,
- L inductance per unit length of series elements,
- C capacitance per unit length of series elements,
- l_m length series elements,
- C_s off-state capacitance of switches,
- Z_0 effective characteristic impedance of complete structure,
- V_0 propagation velocity of complete structure.

Also, we can relate the transmission phase shift per section $\theta/2$ (where θ is the phase increment required of the complete circuit) to the propagation velocity

$$\frac{\theta}{2} \cdot \frac{1}{360} = \frac{f}{V_0} \tag{A5}$$

where f is the operating frequency.

Equations (A1)–(A5), with some algebraic manipulation, permit a full solution (if it exists) for a specified requirement. Note that Z_0 is required to be 50 Ω, Z_m has an upper practical limit of ~100 Ω, and V_m is related to Z_m via the geometry and dimensions of the microstrip-line realization.

For a four-bit (22.5° increment) phase shifter at *X*-band, the required values of the unknowns are thus calculated

to be

switch off-state capacitance	C_s	0.05 pF
series element characteristic impedance	Z_m	100 Ω
series element length	l_m	0.017 wavelengths.

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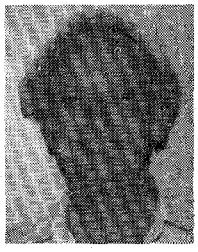
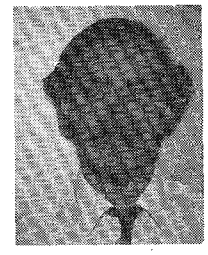


Ken Wilson was born within the sound of Bow Bells in London, England. After two years of service in the Royal Air Force, he joined the GEC Research Limited, Hirst Research Centre, in 1955. Following part-time study at London University, he graduated with a first class honors degree in electrical engineering.

His career has been devoted to design, assessment, and applications of advance semiconductor devices, and he initiated the MMIC programs at the GEC in 1980. He is currently a Senior Group Leader in the Compound Semiconductor Division.



Jonathan M. C. Nicholas was born in 1960 in Sussex, England, and in 1981 obtained a first class honors degree in physics at Christ Church, Oxford.

In the same year, he joined the GEC Research Limited, Hirst Research Centre, to work on design and assessment of GaAs FET's and monolithic circuits. In 1983, he was made a Group Leader in the Compound Semiconductor Laboratory responsible for microwave assessment. He now leads the MMIC design group.

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Gary McDermott was born in London, England, on October 5, 1960. He received a B.Sc. with first honors in physics from the University of Aston in Birmingham, England, and a diploma in microwave engineering and an M.S.c. in microwave and modern optics from the University College London, England.

From 1981 to 1982, he worked at the GEC Research Limited, Hirst Research Centre, on the development of a beam-lead silicon p-i-n diode as part of his undergraduate training. Since 1983, he has worked at the same establishment in the Compound Semiconductor Laboratory on the fabrication of discrete GaAs devices and MMIC's.

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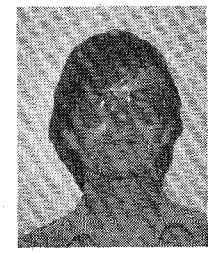

John W. Burns was born in Lancashire, England, in 1959. He received an honors degree in electrical and electronic engineering from the Polytechnic of Newcastle-upon-Tyne, England, in 1981.

He joined the GEC Research Limited, Hirst Research Centre, in the summer of the same year and initially spent two years working on the design of millimeter-wave radar components. This was followed by one year involved in the development of IMPATT technology at millimeter-wave frequencies. In April 1984 he was appointed Group Leader of the Microwave Assessment group within the Compound Semiconductor Laboratory at the Hirst Research Centre, responsible for all aspects of RF measurement and diagnostics related to GaAs components and MMIC's. He is a Member of the Institution of Electrical Engineers (Great Britain).